CLAIMS

What is claimed is:

1. An analog to digital conversion system, comprising:

a plurality of cascaded successive approximation subconverter stages, each subconverter stage receiving a subconverter stage analog input signal and providing a subconverter stage digital output signal representative of the subconverter stage analog input signal, the plurality of successive approximation subconverter stages individually comprising:

a switched capacitor system receiving an analog subconverter stage input voltage at a switched capacitor system input node and receiving a thermometer coded intermediate digital signal, the switched capacitor system providing an analog switched capacitor system output signal at a switched capacitor system output node, wherein the switched capacitor system comprises:

a plurality of capacitors having substantially equal capacitance values, individual capacitors comprising a first terminal and a second terminal; and

a switching system coupled to the second terminals of the plurality of capacitors, the switching system selectively coupling individual capacitors to one of the switched capacitor system input node, the switched capacitor system output node, a first reference voltage, and a second reference voltage according to the thermometer coded intermediate digital signal.

2. The analog to digital conversion system of claim 1, wherein:

in a sample mode, the switched capacitor system stores the subconverter stage input voltage in the plurality of capacitors;

in a conversion mode, the switched capacitor system applies the intermediate digital signal to the plurality of capacitors and provides the switched capacitor system output signal representative of a difference between the

subconverter stage input voltage and a value of the intermediate digital signal; and

in a residue amplification mode, the switched capacitor system provides the switched capacitor system output signal representative of a difference between the subconverter stage input voltage and a final value of the intermediate digital signal.

3. The analog to digital conversion system of claim 1, wherein the analog to digital conversion system receives a differential conversion system analog input signal, wherein the individual switched capacitor systems receive a differential analog subconverter stage input voltage at first and second switched capacitor system input nodes and provide a differential analog switched capacitor system output signal at first and second switched capacitor system output nodes, and wherein the switched capacitor systems individually comprise:

a first plurality of capacitors individually comprising a first terminal and a second terminal coupled to the switching system; and

a second plurality of capacitors individually comprising a first terminal and a second terminal coupled to the switching system.

4. The analog to digital conversion system of claim 1, wherein the subconverter stages individually further comprise:

an amplifier system coupled with the switched capacitor system, the amplifier system amplifying the switched capacitor system output signal and providing an analog subconverter stage residue output signal according to the switched capacitor system output signal;

a comparison system coupled with the amplifier system and providing a comparison signal according to the switched capacitor system output signal; and

a successive approximation system coupled with the switched capacitor system and the comparison system, the successive approximation system

providing the thermometer coded intermediate digital signal and a subconverter stage digital output signal according to the comparison signal;

wherein in the conversion mode, the successive approximation system iteratively adjusts the value of the thermometer coded intermediate digital signal according to the comparison signal; and

wherein in the residue amplification mode, the amplifier system amplifies the switched capacitor system output signal by a gain factor using at least one capacitor from the plurality of capacitors to provide an analog subconverter stage residue output signal.

5. The analog to digital conversion system of claim 4, wherein a first subconverter stage receives a conversion system analog input signal as the subconverter stage input voltage, wherein the successive approximation system provides a J-bit subconverter stage digital output signal, J being an integer greater than 1, and wherein the gain factor for the first subconverter stage is less than $2^{(J-1)}$.

6. The analog to digital conversion system of claim 5, wherein a second subconverter stage receives an analog subconverter stage residue output signal from the first subconverter stage, wherein the successive approximation system of the second subconverter stage provides a K-bit subconverter stage digital output signal, K being an integer greater than 1, and wherein the gain factor for the second subconverter stage is greater than $2^{(K-1)}$.

7. The analog to digital conversion system of claim 4, wherein the analog to digital conversion system receives a differential conversion system analog input signal, wherein the individual switched capacitor systems receive a differential analog subconverter stage input voltage at first and second switched capacitor system input nodes and provide a differential analog switched capacitor

system output signal at first and second switched capacitor system output nodes, and wherein the switched capacitor systems individually comprise:

a first plurality of capacitors individually comprising a first terminal and a second terminal coupled to the switching system; and

a second plurality of capacitors individually comprising a first terminal and a second terminal coupled to the switching system.

8. The analog to digital conversion system of claim 4, wherein the switched capacitor systems individually further comprise a mode control system coupled with the switching system, the mode control system providing thermometer coded control signals to the switching system to selectively couple individual capacitors to one of the switched capacitor system input node, the switched capacitor system output node, the first reference voltage, and the second reference voltage in the sample, conversion, and residue amplification modes.

9. The analog to digital conversion system of claim 8, wherein at least one of the capacitors is coupled with the switched capacitor system input node in the sampling mode, with one of the first and second reference voltages in the conversion mode, and with the switched capacitor system output node in the residue amplification mode.

10. The analog to digital conversion system of claim 1, wherein a first subconverter stage receives a conversion system analog input signal as the subconverter stage input voltage, wherein a first subconverter stage provides a J-bit subconverter stage digital output signal, J being an integer greater than 1, wherein in a residue amplification mode, the first subconverter stage amplifies the switched capacitor system output signal by a gain factor using at least one capacitor from the plurality of capacitors to provide an analog subconverter stage

residue output signal, and wherein the gain factor for the first subconverter stage is less than $2^{(J-1)}$.

11. The analog to digital conversion system of claim 10, wherein a second subconverter stage receives an analog subconverter stage residue output signal from the first subconverter stage, wherein the second subconverter stage provides a K-bit subconverter stage digital output signal, K being an integer greater than 1, wherein the second subconverter stage amplifies the switched capacitor system output signal by a gain factor using at least one capacitor from the plurality of capacitors to provide an analog second subconverter stage residue output signal, and wherein the gain factor for the second subconverter stage is greater than $2^{(K-1)}$.

12. The analog to digital conversion system of claim 1, further comprising a digital error correction system coupled to the subconverter stages and receiving subconverter stage digital output signals from the subconverter stages, the error correction system providing a conversion system digital output signal according to the subconverter stage digital output signals.

13. A pipelined analog to digital conversion system, comprising:

a first successive approximation subconverter stage comprising a first capacitor array, the first successive subconverter stage receiving a conversion system analog input and providing a first multi-bit subconverter stage digital output representative of the conversion system analog input and a first residue output representative of a difference between the conversion system analog input and the first subconverter stage digital output; and

a second successive approximation subconverter stage comprising a second capacitor array, the first successive subconverter stage receiving the first

residue output and providing a second multi-bit subconverter stage digital output representative of the first residue output.

14. The conversion system of claim 13, wherein the first capacitor array comprises a first plurality of capacitors having substantially equal capacitance values, each comprising a first terminal coupled to a first capacitor array intermediate node, and a second terminal, and wherein the first subconverter stage further comprises a switching system coupled to the second terminals of the plurality of capacitors, the switching system selectively coupling individual capacitors to one of a first capacitor array input node, a first capacitor array output node, a first reference voltage, and a second reference voltage according to a thermometer coded intermediate digital signal.

15. The conversion system of claim 13, wherein the first subconverter stage provides a J-bit subconverter stage digital output, J being an integer greater than 1, wherein in a residue amplification mode, the first subconverter stage amplifies the conversion system analog input by a first gain factor to provide the first residue output, and wherein the first gain factor is less than $2^{(J-1)}$.

16. The conversion system of claim 15, wherein the second subconverter stage provides a K-bit subconverter stage digital output, K being an integer greater than 1, wherein the second subconverter stage amplifies the first residue output by a second gain factor to provide an analog second subconverter stage residue output signal, and wherein the second gain factor is greater than $2^{(K-1)}$.

17. The conversion system of claim 15, wherein the analog to digital conversion system receives a differential conversion system analog input, and wherein the individual subconverter stages receive a differential analog

subconverter stage input voltage at first and second input nodes and provide a differential analog subconverter stage output at first and second subconverter stage output nodes.

18. The conversion system of claim 15, further comprising a digital error correction system coupled to the subconverter stages and receiving the multi-bit subconverter stage digital outputs from the subconverter stages, the error correction system providing a conversion system digital output signal according to the subconverter stage digital outputs.